

**REMARKS**

Claims 1-7 and 11-15, 18-19 and 21-23 are pending in the application. Claims 1, 6-7, 12-13, 15, 18-19 and 21 have been amended. Claims 8-9, 16-17 and 20 have been canceled. In view of the following, all of the claims are in condition for allowance. If, after considering this response, the Examiner does not agree that all of the claims are allowable, then the Examiner is requested to schedule a teleconference with the Applicant's attorney to further the prosecution of the application.

**Rejection of claims 1-7, 11-15, 18-19 and 21-23 under 35 U.S.C. 103(a) as being unpatentable over Takinosawa (US 6,977,960) in view of Fan et al. (US 2004/0030968)**

**Claim 1**

Claim 1, as amended, recites a transmit register that comprises a register array and generates a programmable combination of a plurality of bit sequences, each of the bit sequences stored in the register array.

For example, referring, e.g., to FIGS. 4 and 5 and paragraphs 34-38 of the present application, a transmit register 90 (or 100) comprises a register array 92 (or 104) and generates a programmable combination of a plurality of bit sequences, each of the bit sequences stored in the register array. By using a pointer 94 (or 106) to point to different bit sequences in the register array 92 (or 104), it is possible to send any number of combinations of bit sequences in any order to the SERDES circuits 14.

Takinosawa, on the other hand, does not teach a transmit register that comprises a register array and generates a programmable combination of a plurality of bit sequences, each of the bit sequences stored in the register array. Instead, Takinosawa simply teaches a BIST circuit 35 having a pseudo random number generator 61. The Examiner concedes on page 4 of the Office Action that Takinosawa fails to teach an error detector that is coupled to the transmit register. In addition, the Examiner also concedes on page 6 of the Office Action that Takinosawa fails to teach a transmit register comprising a register array.

Similarly, Fan does not teach a transmit register that comprises a register array and generates a programmable combination of a plurality of bit sequences, each of the bit sequences stored in the register array. The Examiner concedes on page 6 of the Office Action that Fan fails to teach a transmit register comprising a register array.

The Examiner mistakenly claims on page 6 of the Office Action that Chen et al. (US 5,726,991) teaches a transmit register comprising a register array. Instead, Chen simply teaches a bit test pattern generator 36 (col. 3, line 65 to col. 4, line 6). The bit test pattern may be fixed (stored in a ROM or a register) or pseudo-random (generated by a sequence of flip flops or created by a software program) (col. 4, lines 2-6). However, storing a fixed bit test pattern in a single ROM/register has nothing to do with generating a programmable combination of a plurality of bit sequences where each of the bit sequences is stored in a register array. In fact, after reviewing Chen in its entirety, the Applicant's attorney is unable to find any mention of a transmit register having a register array storing a plurality of bit sequences. Furthermore, the Applicant's attorney is unable to find any mention of generating a programmable combination of a plurality of bit sequences.

Therefore, the combination of Takinosawa, Fan and Chen do not satisfy the limitations of claim 1.

#### **Claims 12, 18 and 21**

Claims 12, 18 and 21, as amended, are patentable for reasons similar to those recited above in support of the patentability of claim 1.

#### **Claims 2-7, 11, 13-15, 19 and 22-23**

Claims 2-7, 11, 13-15, 19 and 22-23 are patentable by virtue of their respective dependencies from independent claims 1, 12, 18 and 21.

### CONCLUSION

In light of the foregoing remarks, claims 1-7 and 11-15, 18-19 and 21-23 are in condition for allowance, which is respectfully requested.

In the event additional fees are due as a result of this amendment, you are hereby authorized to charge such payment to Deposit Account No. 07-1897.

If, after considering this response, the Examiner does not agree that all of the claims are allowable, then it is respectfully requested that the Examiner contact the Applicant's attorney at (425) 455-5575.

DATED this 2<sup>nd</sup> day of October, 2006.

Respectfully submitted,

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A handwritten signature in black ink, appearing to read "J. Mark Han", is written over a horizontal line.

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